



S/N 10/075484

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Arup Bhattacharyya	Examiner:	Trong Phan
Serial No.:	10/075484	Group Art Unit:	2818
Filed:	February 12, 2002	Docket:	1303.043US1
Title:	ASYMMETRIC BAND-GAP ENGINEERED NONVOLATILE MEMORY DEVICE		

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

INFORMATION DISCLOSURE STATEMENT

Serial No :10/075484

Filing Date: February 12, 2002

Title: ASYMMETRIC BAND-GAP ENGINEERED NONVOLATILE MEMORY DEVICE

Page 2
Dkt: 1303.043US1

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

ARUP BHATTACHARYYA

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6960

Date 2-18-04

By M L B
Marvin L. Beekman
Reg. No. 38,377

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 18th day of February, 2004.

Name

Amy Moriarty

Signature

[Signature]

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number 10/075484

Filing Date February 12, 2002

First Named Inventor Bhattacharyya, Arup

Group Art Unit 2818

Examiner Name Phan, Trong

Sheet 1 of 3

Attorney Docket No: 1303.043US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-2003/0042527	03/06/2003	Forbes, Leonard , et al.	257	315	08/30/2001
	US-2003/0042532	03/06/2003	Forbes, Leonard	257	316	08/30/2001
	US-2003/0043622	03/06/2003	Forbes, Leonard	365	185.05	08/30/2001
	US-2003/0043630	03/06/2003	Forbes, Leonard , et al.	365	185.26	08/30/2001
	US-2003/0043632	03/06/2003	Forbes, Leonard	365	185.28	08/30/2001
	US-2003/0043633	03/06/2003	Forbes, Leonard , et al.	365	185.28	12/20/2001
	US-2003/0043637	03/06/2003	Forbes, Leonard , et al.	365	185.33	08/30/2001
	US-2003/0045082	03/06/2003	Eldridge, Jerome M., et al.	438	593	02/20/2002
	US-2003/0048666	03/13/2003	Eldridge, Jerome M., et al.	365	185.28	06/21/2002
	US-2004/0004245	01/08/2004	Forbes, Leonard , et al.	257	315	07/08/2002
	US-2004/0004247	01/08/2004	Forbes, Leonard , et al.	257	324	07/08/2002
	US-2004/0004859	01/08/2004	Forbes, Leonard , et al.	365	185.05	07/08/2002
	US-3,978,577	09/07/1976	Bhattacharyya, Arup , et al.	29	571	06/30/1975
	US-4,412,902	11/01/1983	Michikami, Osamu , et al.	204	192	06/18/1982
	US-4,780,424	10/25/1988	Holler, Mark A.	437	29	09/28/1987
	US-5,350,738	09/27/1994	Hase, Takashi , et al.	505	473	11/27/1992
	US-5,691,230	11/25/1997	Forbes, Leonard	437	62	09/04/1996
	US-5,801,401	09/01/1998	Forbes, Leonard	257	77	01/29/1997
	US-5,936,274	08/10/1999	Forbes, Leonard , et al.	257	315	07/08/1997
	US-5,952,692	09/14/1999	Nakazato, Kazuo , et al.	257	321	10/28/1997
	US-5,981,350	11/09/1999	Geusic, Joseph E., et al.	438	386	05/29/1998
	US-6,025,627	02/15/2000	Forbes, Leonard , et al.	257	321	05/29/1998

EXAMINER**DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

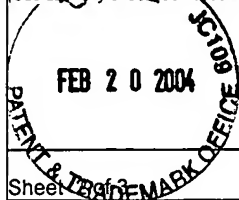
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Complete if Known

Application Number	10/075484
Filing Date	February 12, 2002
First Named Inventor	Bhattacharyya, Arup
Group Art Unit	2818
Examiner Name	Phan, Trong

Attorney Docket No: 1303.043US1

	US-6,031,263	02/29/2000	Forbes, Leonard , et al.	257	315	07/29/1997
	US-6,134,175	10/17/2000	Forbes, Leonard , et al.	365	230.06	08/04/1998
	US-6,143,636	11/07/2000	Forbes, Leonard , et al.	438	587	08/20/1998
	US-6,208,164	03/27/2001	Noble, Wendell P., et al.	326	41	08/04/1998
	US-6,475,857	11/05/2002	Kim, Woosik , et al.	438	240	06/21/2001

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
--------------------	---------------------	------------------	---	-------	----------	----------------

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		ARYA, S. , et al., "Conduction Properties of Thin Al ₂ O ₃ Films", <u>Thin Solid Films</u> , 91, (1982),363-374	
		BHATTACHARYYA, A. , "Physical & Electrical Characteristics of LPCVD Silicon Rich Nitride", <u>ECS Technical Digest</u> , J. Electrochem. Soc., 131(11), 691 RDP, New Orleans, (1984),469C	
		DIPERT, BRIAN , "Flash Memory Goes Mainstream", <u>IEEE Spectrum</u> , 30(10), (October 1993),48-52	
		ELDRIDGE, J. M., et al., "Growth of Thin PbO Layers on Lead Films", <u>Surface Science</u> , 40, (1973),512-530	
		ELDRIDGE, J. , et al., "Measurement of Tunnel Current Density in a Metal-Oxide-Metal System as a Function of Oxide Thickness", <u>Proc. 12th Intern. Conf. on Low Temperature Physics</u> , (1971),427-428	
		GREINER, J. , "Josephson Tunneling Barriers by rf Sputter Etching in an Oxygen Plasma", <u>Journal of Applied Physics</u> , 42(12), (November 1971),5151-5155	
		GREINER, J. , "Oxidation of lead films by rf sputter etching in an oxygen plasma", <u>Journal of Applied Physics</u> , 45(1), (1974),32-37	
		GUNDLACH, K. , et al., "Logarithmic Conductivity of Al-Al ₂ O ₃ -Al Tunneling Junctions Produced by Plasma and by Thermal Oxidation", <u>Surface Science</u> , 27, (1971),125-141	
		HAN, KWANGSEOK , "Characteristics of P-Channel Si Nano-Crystal Memory", <u>IEDM Technical Digest</u> , International Electron Devices Meeting, (December 10-13, 2000),309-312	
		HURYCH, Z. , "Influence of Non-Uniform Thickness of Dielectric Layers on Capacitance and Tunnel Currents", <u>Solid-State Electronics</u> , vol. 9, (1966),967-979	
		INUMIYA, S , et al., "Conformable formation of high quality ultra-thin amorphous	

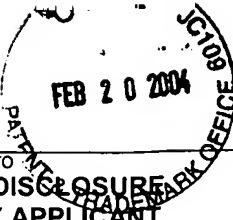
EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

FEB 20 2004



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number	10/075484
Filing Date	February 12, 2002
First Named Inventor	Bhattacharyya, Arup
Group Art Unit	2818
Examiner Name	Phan, Trong

Sheet 3 of 3

Attorney Docket No: 1303.043US1

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Ta2 O5 gate dielectrics utilizing water assisted deposition (WAD) for sub 50 nm damascene metal gate MOSFETs", <u>IEDM Technical Digest. International Electron Devices Meeting</u> , (December 10-13, 2000),649-652	
		KUBASCHEWSKI, O. , et al., "Oxidation of Metals and Alloys", <u>Butterworths</u> , London, (1962),53-63	
		LUAN, H. F., "High Quality Ta2O5 Gate Dielectrics with Tox,eq<10A", <u>IEDM Technical Digest. International Electron Devices Meeting</u> , (December 5-8, 1999),141-143	
		MANCHANDA, L. , "Si-doped aluminates for high temperature metal-gate CMOS: Zr-Al-Si-O, a novel gate dielectric for low power applications", <u>IEDM Technical Digest. International Electron Devices Meeting</u> , (December 10-13, 2000),23-26	
		MASUOKA, F. , et al., "A 256K Flash EEPROM using Triple Polysilicon Technology", <u>IEEE International Solid-State Circuits Conference, Digest of Technical Papers</u> , (1985),168-169	
		MASUOKA, F. , et al., "A New Flash EEPROM Cell using Triple Polysilicon Technology", <u>International Electron Devices Meeting, Technical Digest</u> , San Francisco, CA,(1984),464-467	
		MORI, S. , et al., "Reliable CVD Inter-Poly Dielectrics for Advanced E&EEPROM", <u>Symposium on VLSI Technology, Digest of Technical Papers</u> , (1985),16-17	
		PASHLEY, R. , et al., "Flash Memories: the best of two worlds", <u>IEEE Spectrum</u> , 26(12), (December 1989),30-33	
		POLLACK, S. , et al., "Tunneling Through Gaseous Oxidized Films of Al2O3", <u>Transactions of the Metallurgical Society of AIME</u> , 233, (1965),497-501	
		ROBERTSON, J. , et al., "Schottky Barrier height of Tantalum oxide, barium strontium titanate, lead titanate, and strontium bismuth tantalate", <u>Applied Physics Letters</u> , vol. 74, no. 8, (02/22/1999),1168-1170	
		SHI, YING , "Tunneling Leakage Current in Ultrathin (<4 nm) Nitride/Oxide Stack Dielectrics", <u>IEEE Electron Device Letters</u> , 19(10), (October 1998),388-390	
		SIMMONS, J. , "Generalized Formula for the Electric Tunnel Effect between Similiar Electrodes Separated by a Thin Insulating Film", <u>Journal of Applied Physics</u> , 34(6), (1963),1793-1803	
		SZE, S. , "Physics of Semiconductor Devices, Second Edition", <u>John Wiley & Sons</u> , New York, (1981),553-556	
		YAMAGUCHI, TAKESHI , "Band Diagram and Carrier Conduction Mechanism in ZrO2/Zr-silicate/Si MIS Structure Fabricated by Pulsed-laser-ablation Deposition", <u>Electron Devices Meeting, 2000. IEDM Technical Digest. International</u> , (2000),19-22	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached